

# David Jeffrey Ljung Madison

## Programming, Algorithm Design/Development, VLSI / CPU Verification

### Version Info

Resume v4.5, released 2014-04-01.

Please get current source at: <http://DaveSource.com/Resume/>

### Contact Info

Before contacting me, make sure you have an up-to-date resume.

**I am not interested in full-time work unless it is flexible, and I am not interested in long-term relocating.**

Recruiters: Use email, **DO NOT CALL**

Home: 415.341.5555 (call between 11a-8p PST)

Email: [resumeMail@DaveSource.com](mailto:resumeMail@DaveSource.com)

### Work Experience

*Director of Verification, [iCelero, LLC](#). Jul 2007 - Dec 2013.*

- Managed verification for a complex, fully-custom processor under a very tight schedule
- Created complete toolchain and testbenches for [entire CPU verification process](#), from block level to full-chip to SOC.
- Created highly sophisticated test packer/generator for VLIW CPU

*Independent Consultant, [DaveSource Consulting](#). Jul 2002 - Present.*

Contractor for VLSI/Processor Verification and/or software design/implementation.

- CPU verification, formal verification tool design.
- Designed and implemented operations management algorithms. Order of magnitude improvement in runtime **and** savings.
- Custom image sorting software, custom web apps.

*CPU Verification Engineer, [Transmeta Corp](#). Jan 2000 - Jul 2002.*

- Created cycle-accurate models (verilog, perl, scheme) of blocks
- Wrote pseudo-directed random test generators (verilog, scheme).
- Due to original formal verification techniques on blocks, [all bugs were found pre-silicon](#).

*CPU Verification Engineer, [SandCraft Inc.](#). Jul 1998 - Jan 2000.*

In charge of initial verification of the execute half of [SRI/Montage](#) CPU:

- Designed modular verilog/PLI testbench for blocks/fullchip, verified blocks
- Created majority of verification tool environment.

*CPU Verification and Debug, [VLSI Technology Lab](#), [Hewlett-Packard](#). Aug 1994 - Jun 1998.*

Post-silicon debug/tools:

- Created the entire tool chain from scratch (except for some random code generators), including boot code and test framework, controller/environment scripts, shmoo scripts, fail search/eval, etc..

- Hardware environmental testing and debug software
- Finding and debugging failures

Pre-silicon verification:

- Random code generators, test creation
- Test checkers and evaluators
- Tools writer

Other duties:

- Lab Resource: Unix, programming, scripting..
- Tool geek (wrote CAD tools, personnel tools, etc..)

*Shareware Programmer, [Marginal Hacks](#)*

I wrote many popular tools at [Marginal Hacks](#), including the highly popular [album](#) software.

## Publications

- [CPU electrical verification](#), August 1997, [HP Journal](#) (as "David J. Ljung") [[local copy](#)]
- [CPU Block verification using formal tools](#)

## Skills

*Computer Languages*

Fluent in C, Ruby, Perl, Java, Scheme, Verilog and many versions of Assembly. I often become the perl guru/resource wherever I work. I can do C++, but I'm not a fan.

Experience with: Lisp, Python, Basic, Fortran, sed, yacc, sh, ksh, zsh, csh, tcsh, etc..

[Breaking things](#)

I like to use things in new and interesting ways, this is one of the things that sets me out as a verification engineer. I have managed to break and find bugs in almost every tool I have used, such as:

gcc, cpp preprocessor, HP-UX CC, HP-UX linker, various assemblers, perl (2 so far), various shells (tcsh, ksh, ..), verilog simulators (VCS, ESP), rccs, etc..

## Education

**Degree:** B.S. ECE/CS (Double major: [Electrical Computer Engineering](#) with Computer Option and [Computer Science](#))

**School:** 1989-1994: [University Of Wisconsin, Madison](#)

[Time's Person of the Year](#), 2006